REMARKS

Claims 44-73 are presently pending. Claims 44-47, 49-52, 54-61, 63-69, and 71-73 were rejected. Claims 48, 53, 62, and 70 were objected to but indicated as allowable if rewritten in independent form. Assignee thanks Examiner for indication of allowable subject matter.

Claims 44, 49, 57, and 66 were rejected under 35 U.S.C. 103(a) as obvious from Furuyama, obvious from Wendell, and obvious from Saruwatari.

Examiner indicated that "Furuyama et al (see Fig. 8) shows an addressing means for providing redundancy decoding that includes a plurality of predecoder (50, 51, 52) based on the coupled address bits (A0-A2, A3-A4, A5-A7, respectively). Thus, based on the supplied address bits, each corresponding predecoder is activated or selected and their outputs is coupled to the main decoder (53), and thus it would have been obvious to one skilled in this art that when/if decoder is selected, it's predecoded address input lines are also shifted into work, and the other two decoders are shifted out as inactive or idles states. For example, in Figure 12 shows in detail the structure of predecoder (50) ... however, the analogous use of particular applied address bits (upper and lower 3 bits) in this reference obviously acting as 'control" bits for activating or "shifting in" only one predecoder's address lines for active use while still be able to deactivating or "shifting out" the other predecoder lines from the two non=active predecoders based on supplied address bits."

Assignee respectfully traverses and disagrees with Examiner's characterization of Furuyama, particularly of the coupled address bits (A0-A7) as "control bits for activating or shifting in only one predecoder's address lines..." and call Examiner's attention to Furuyama, col. 7, Lines 54-59 ("The column address decoder 22 is provided with a first predecoder 50 for receiving low-order three bit address signals A0 to A2 of eight-bit column address signals, a second predecoder 51 for receiving middle-order two-bit address signals A3 and A4, and a third predecoder 52 for receiving high-order three-bit address signals A5 to A7. ... The main decoder 53 outputs 256 (=8x4x8) column selection signals obtained by combining predecode signals supplied from the first to third predecoders 50 to 52 to each memory cell array 20." (Emphasis Added).

Accordingly, Furuyama does not teach or fairly suggest "shifting in" or "shifting out" a "predecoder", and Examiner is requested to withdraw this rejection.

Examiner indicated that "Wendell et al (see Fig. 4) shows an addressing means for providing redundancy decoding that includes a plurality of predecoder (410, 411,412) based on the coupled address bits (RA0 to RA7, respectively). Thus, based on the supplied address bits, each corresponding predecoder is activated or selected and their outputs is coupled to the main row decoder (201), and thus it would have been obvious to one skilled in this art that when/if decoder is selected, it's predecoded address input lines are also shifted into work, and the other two decoders are shifted out as inactive or idles states. For example, in Figure 4 shows in detail the structure of address shifting circuitry (using NOT comparators 402 and AND gate 405) in order to activate or shift in a proper predecoder to be used (based on the supplied input address bits (A0 to A2)). ... however, the analogous use of particular applied address bits (upper and lower 3 bits) in this reference obviously acting as 'control" bits for activating or "shifting in" only one predecoder's address lines for active use while still be able to deactivating or "shifting out" the other predecoder lines from the two non-active predecoders based on supplied address bits."

Assignee respectfully traverses and disagrees with Examiner's characterization of Wendell. Examiner provides no citation to Wendell that even indicates that any predecoder is deactivated. Moreover, Assignee has reviewed Wendell and submits that Wendell does not teach or fairly suggest this. Accordingly, Wendell does not teach or fairly suggest the claimed "shifting in" or "shifting out" a "predecoder", and Examiner is requested to withdraw this rejection.

Examiner indicated that "Saruwatari et al (see Fig. 3) shows an addressing means for providing redundancy decoding that includes a plurality of predecoder (14a, 14b, 15) based on the coupled address bits (Y1 to Y4, respectively). Thus, based on the supplied address bits, each corresponding predecoder is activated or selected (by the shown program circuit 15a) and their respective outputs is coupled to the main decoders (RDC or DC1-32)..."

Assignee respectfully traverses and disagrees with Examiner's characterization of Saruwatari. Examiner provides no citation to Wendell that even indicates that any predecoder is deactivated. Moreover, Assignee has reviewed Saruwatari and submits that Saruwatari does not teach or fairly suggest this. Accordingly, Saruwatari does not teach or fairly suggest the claimed "shifting in" or "shifting out" a "predecoder" and Examiner is requested to withdraw this rejection.

Conclusion

For at least the foregoing reasons, claims 44, 49, 57, and 66 are allowable, as well as dependent claims 45-48, 50-56, 58-65, and 67-73. Accordingly, the Application is in a condition for allowance and Examiner is requested to pass this case to issuance.

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Respectfully submitted,

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